PATENT APPLICATION
DOCKET NO.: 10010788-1

LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the claims, claims 1-29, of the present patent application.

1. (Previously Presented) A system for synchronizing a first circuit portion operating in a first clock domain that is clocked with a first clock signal and a second circuit portion operating in a second clock domain that is clocked with a second clock signal, comprising:

means for generating a SYNC pulse signal based on occurrence of a coincident edge between said first and second clock signals; and

a clock synchronizer controller operable to generate a plurality of control signals based on said SYNC pulse signal, said clock synchronizer controller including a SYNC adjuster operable to re-position said SYNC pulse signal based on a new coincident edge between said first and second clock signals defined in response to a skew between said first and second clock signals, wherein at least a portion of said plurality of control signals actuate data transfer synchronizer circuitry disposed between said first and second circuit portions.

2. (Currently Amended) The system as set forth in claim 1, wherein said SYNC adjustor comprises:

a SYNC correct block operable to receive said SYNC pulse signal via a SYNC distributor, said SYNC correct block for correcting said SYNC pulse signal if said SYNC pulse signal has a particular clock period difference with respect to said first clock signal;

a ratio detector coupled to said SYNC correct block for detecting a frequency ratio relationship between said first and second clock signals;

a state/correct block associated with a phase detector for determining a state indicative of a phase difference between said first and second clock signals, said state/correct block operating responsive to said frequency ratio relationship detected by said ratio detector; and

a skew compensator operating responsive to said state to redefine [[a]] <u>said</u> new coincident rising edge with respect to said first and second clock signals, whereby said SYNC pulse signal is re-aligned so as to correspond with said new coincident rising edges of said first and second clock signals.

3. (Original) The system as set forth in claim 2, further comprising a tapline and selection block operable to drive said plurality of control signals at predetermined times based on said SYNC pulse signal.

4. (Original) The system as set forth in claim 3, wherein said SYNC distributor comprises a plurality of registers.

5. (Original) The system as set forth in claim 3, wherein said data transfer synchronizer circuitry comprises at least one of a CLK1-TO-CLK2 synchronizer operable to facilitate data transmission from said first circuit portion to said second circuit portion and a CLK2-TO-CLK1 synchronizer operable to facilitate data reception by said first circuit portion from said second circuit portion.

6. (Original) The system as set forth in claim 5, wherein said plurality of control signals comprises a CLK1-TO-CLK2_VALID signal provided to said first circuit portion and an NDSYNC signal operable to actuate said CLK1-TO-CLK2 synchronizer.

7. (Original) The system as set forth in claim 5, wherein said plurality of control signals comprises a CLK2-TO-CLK1_VALID signal provided to said first circuit portion and an NRSYNC signal operable to actuate said CLK2-TO-CLK1 synchronizer.

8. (Original) The system as set forth in claim 5, wherein each of said CLK1-TO-CLK2 and CLK2-TO-CLK1 synchronizers includes a set/reset asynchronous flip-flop.

9. (Original) The system as set forth in claim 5, wherein said tapline and selection block comprises a plurality of delay registers.

10. (Original) The system as set forth in claim 5, wherein each of said plurality of control signals is staged through at least a flip-flop.

11. (Previously Presented) A method of synchronizing data transfer operations between two circuit portions across a clock domain boundary, comprising:

generating a secondary clock signal from a primary clock signal, wherein said primary clock signal is operable to clock a first circuit portion and said secondary clock signal is operable to clock a second circuit portion;

generating a SYNC pulse signal based on occurrence of a coincident edge between said primary and secondary clock signals;

adjusting said SYNC pulse signal to re-position it based on a new coincident edge that is defined responsive to a skew between said primary and secondary clock signals; and

generating data transfer control signals at appropriate times relative to said primary and secondary clock signals based on said SYNC pulse signal to control data transfer operations between said first and second circuit portions.

12. (Original) The method as set forth in claim 11, wherein said secondary clock signal is generated by a phase-locked loop (PLL) based on said primary clock signal.

13. (Original) The method as set forth in claim 11, wherein said SYNC pulse signal is generated when a rising edge in said primary clock signal coincides with a rising edge in said secondary clock signal.

14. (Original) The method as set forth in claim 11, wherein said SYNC pulse signal is corrected if said SYNC pulse signal has a select clock period difference with respect to said primary clock signal.

15. (Currently Amended) The method as set forth in claim 11, further comprising:

determining a state indicative of a phase difference between said primary and secondary clock signals; and

redefining [[a]] <u>said</u> new coincident rising edge with respect to said primary and secondary clock signals based on said state.

16. (Original) The method as set forth in claim 15, wherein said new coincident rising edges with respect to said primary and secondary clock signals are redefined by adding at least an extra clock cycle when said state indicates that said primary clock signal lags with respect to said secondary clock signal by a predetermined amount.

17. (Original) The method as set forth in claim 15, wherein said new coincident rising edges with respect to said primary and secondary clock signals are redefined by deleting at least an extra clock cycle when said state indicates that said secondary clock signal lags with respect to said primary clock signal by a predetermined amount.

18. (Original) The method as set forth in claim 11, wherein said data transfer control signals are staged through a plurality of registers before being provided to data transfer synchronizer circuitry disposed between said first and second circuit portions.

19. (Original) The method as set forth in claim 11, wherein said primary clock signal comprises a core clock in a computer system.

20. (Original) The method as set forth in claim 19, wherein said secondary clock signal comprises a bus clock in a computer system.

21. (Previously Presented) A method of synchronizing data transfer operations between two circuit portions across a clock domain boundary, comprising:

generating a SYNC pulse signal based on occurrence of a coincident edge between a primary clock signal operable with a first clock domain and a secondary clock signal operable with a second clock domain;

compensating for a skew between said primary and secondary clock signals and adjusting said SYNC pulse signal to re-position it based on said skew, if necessary, wherein said compensating includes (i) determining a state indicative of a phase difference between said primary and secondary clock signals, and (ii) redefining a new coincident edge with respect to said primary and secondary clock signals based on said state; and

generating data transfer control signals at appropriate times relative to said primary and secondary clock signals based on said SYNC pulse signal to control data transfer operations between said two circuit portions.

22. (Previously Presented) The method as set forth in claim 21, wherein said secondary clock signal is generated by a phase-locked loop (PLL) based on said primary clock signal.

23. (Previously Presented) The method as set forth in claim 21, wherein said SYNC pulse signal is generated when a rising edge in said primary clock signal coincides with a rising edge in said secondary clock signal.

24. (Previously Presented) The method as set forth in claim 21, wherein said SYNC pulse signal is corrected if said SYNC pulse signal has a select clock period difference with respect to said primary clock signal.

25. (Previously Presented) The method as set forth in claim 21, wherein said new coincident edge with respect to said primary and secondary clock signals comprises a new coincident rising edge redefined by adding at least an extra clock cycle when said state indicates that said primary clock signal lags with respect to said secondary clock signal by a predetermined amount.

26. (Previously Presented) The method as set forth in claim 21, wherein said new coincident edge with respect to said primary and secondary clock signals comprises a new coincident rising edge redefined by deleting at least an extra clock cycle when said state indicates that said secondary clock signal lags with respect to said primary clock signal by a predetermined amount.

27. (Previously Presented) The method as set forth in claim 21, wherein said data transfer control signals are staged through a plurality of registers before being provided to data transfer synchronizer circuitry disposed between said two circuit portions.

28. (Previously Presented) The method as set forth in claim 21, wherein said primary clock signal comprises a core clock in a computer system.

29. (Previously Presented) The method as set forth in claim 28, wherein said secondary clock signal comprises a bus clock in a computer system.